ABSTRACT

Pipelined digital accumulators. Parallel digital accumulators for use in digital signal processing are improved through pipelining. An accumulator is partitioned into a plurality of pipelined stages, and the pipeline delay is used to reduce the effect of carry propagation through the accumulator. While input and output delay registers are used in the accumulator partitions, the output delay registers are not needed if the results of those partitions are not needed in subsequent stages of computation. If phase coherence is not needed, input delay registers may not be needed on accumulator partitions. In the limiting case of one bit per partition, the effective speed of the pipelined accumulator is equivalent to the speed of a single bit accumulator stage.